IN THE SPECIFICATION

Please amend the Specification as follows:

Page 10, line 14, please amend the three paragraphs (Pub. No. 2002/0083354, Para. Nos. 0025-0027) starting there-at and continuing to page 11, line 29 as follows:

"Referring now to Figure 4, waveform diagrams 401-406 illustrate the exemplary functionality of the thermal clock throttling control provided by the present invention. Waveforms 401 and 402 are plotted on an X axis representing an exploded period of time of a clock throttling cycle. Waveform 401 is a temperature waveform corresponding to the right Y axis of Temperature. Waveform 402 is a power waveform corresponding to the left Y axis of Power expanded in time. Waveform 403 illustrates the status of the integrated circuit, such as a processor. Waveform 404 is an exemplary waveform of the force execution stall signal 315. Waveform 405 is an exemplary total activity waveform such as that which would be measured by the thermal activity detector 310. Waveform 406 illustrates the thermal limit 406', a programmed threshold value, which when exceeded by the waveform 405 initiates the sequence of thermal clock throttling provided by the present invention. In the example of Figure 4, the total activity of the integrated circuit exceeds the thermal limit 406' at point 410 on the waveform 405 ~~labeled "~~ during surging processor activity, for example, which is detected [["]].

As illustrated by waveform 403, the integrated circuit 201 experiences a run cycle 411, a response cycle 412 after reaching the thermal limit, a throttling cycle 413 over which the clocks are gradually throttled OFF and then back ON, and a return to a

run cycle 411. The throttling cycle 413 provides a safe frequency transition sequence.

During the throttling cycle 413, the clocks are gradually throttled OFF during a clock throttling period 414, held OFF for a period of time during a hold period 415 and gradually throttled ON during a clock throttling period 416. During clock throttling period 414, the frequency of the clock provided to circuitry is gradually reduced to zero to provide the gradual clock throttling where the clocks are throttled OFF. This is indicated along waveform 402 by the ratio of clock pulses for a given [[give]] period decreasing from N/N to 0/N. During clock throttling period 416, the frequency of the clock provided to circuitry is gradually increased from zero to provide the gradual clock throttling where the clocks are throttled ON. This is indicated along waveform 402 by the ratio of clock pulses for a give period increasing from 0/N to N/N. During the hold period 415, CGCNTL 320 gates the clock CLK 303 by means of the logic gate 307 so that the throttled clock 307 is OFF and has zero frequency. This is indicated along waveform 402 by the ratio of clock pulses for a give period being 0/N. The power consumption indicated during the hold period 415 is a constant typically greater than zero for those circuits that remain being clocked by FCLK 305 and can not be turned OFF using TCLK 307. The throttling cycle 413 may be a function of the activity level."

Page 12, line 3, please amend the paragraph starting there-at (Pub. No. 2002/0083354, Para. No. 0029) as follows:

"During the response cycle 412, a forced execution stall signal 404' is asserted as indicated by waveform 404 and a stall state 418 is entered into where the circuitry and the functional blocks 205 and 207 prepare to have the throttled clock TCLK 307 gradually turned OFF. After the necessary states are saved, the integrated circuit goes into the throttling cycle 413 previously described in detail. After the throttling cycle 413 is completed, the forced execution stall signal 404' is de-asserted and the integrated circuit returns to the run cycle."

Page 17, line 30, please amend the paragraph starting there-at (Pub. No. 2002/0083354, Para. No. 0043) that continues over to page 18, line 28 into two paragraphs as follows:

"Referring now to Figure 6, waveforms 600-616 [[are]] illustrate an exemplary transitioning of the throttling clock signal TCLK 307 to a turned OFF state in response to the thermal clock throttling control of the present invention. The clock waveform is chopped at each stage in waveforms 601-616, reducing the frequency by gating or masking out one clock cycle at each, for example. An interval of time is provided from one stage to the next in order to relax the instantaneous current di/dt.

In waveform 600, throttling clock signal TCLK 307 has a normal clock frequency which is similar to the frequency of the free-running clock FCLK 305. In a given window 620 of a period of time, waveform 600 has sixteen clock pulses 621 in sixteen clock cycles 622 such that N=16. In waveform 600, the clock frequency ratio is N/N=16/16=1. The clock throttling controller

312 of the present invention then reduces the frequency be gating or masking out one clock cycle, such as clock cycle 631, within the given window 620 to reduce the frequency by the ratio of (N-1)/N. In this case, stage 15 of the sixteen stages of the LSFR 510 is selected to mask out (i.e. chop out) the one clock cycle 631. After a period of time for relaxation of the instantaneous current di/dt at this frequency for TCLK 307, a next lower frequency level can be selected. In waveform 602, clock cycles 631 and 632 are masked out to achieve yet another reduction in frequency for TCLK 307. After another period of relaxation in the instantaneous current di/dt, a next lower frequency level can be selected. In waveform 603, clock cycles 631, 632 and 633 are masked out to achieve another gradual reduction in frequency for TCLK 307. This can be continued so on and so forth. In waveform 614 all clock cycles but for clock cycles 645 and 646 are masked out of TCLK 307. In waveform 615 only clock cycle 646 is not masked out of TCLK. Finally, waveform 616 ~~illustrate~~ illustrates TCLK being completely masked out so that it is at a constant level, effectively placing TCLK into an OFF state."